Amendment to the Claims:

Please amend Claims 1, 12 and 15.

Claim 1 (currently amended): An LSI chip having a plurality of output terminals, an internal circuit and a test circuit, the test circuit comprising:

a single test signal input terminal, which receives a test signal, for testing the internal circuit;

a single test signal output terminal, which outputs a test result only;

a shift register having an input terminal, which is connected to the test signal input terminal, output bits of the shift register being equal to a number of the output terminals of the LSI chip, and a voltage level of one of the output bits of the shift register being different from these of other output bits of the shift register in response to a clock pulse; and

a plurality of switches, each of which includes an input terminal, an output terminal and a control terminal, a number of the switches being equal to the number of the output terminals of the LSI chip, each input terminal of the switches being connected to one of the output terminals of the LSI chip, the output terminals of the switches being commonly connected to the test signal output terminal, and each control terminal of each switch being connected to one of the output bits of the shift register.

Claim 2 (original). An LSI chip as claimed in claim 1 wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal.

Claim 3 (original). An LSI chip as claimed in claim 1 further including a clock input terminal, the clock input signal is inputted to the clock input terminal from an external device.

Claim 4 (withdrawn). An LSI chip having a first number of output terminals and a test circuit, the test circuit comprising:

a single test signal input terminal;

a second number of test signal output terminals;

a shift register having an input terminal, which is connected to the test signal input terminal, output bits of the shift register being equal to a third number (integer), which is the first number divided by the second number, and a voltage level of one of the output bits of the shift register being different from these of other output bits of the shift register in response to a clock pulse; and

the third number of switch circuits, each of which includes the second number of input terminals, the second number of output terminals and a single control terminal, each of input terminals of the switch circuits being connected to one of the output terminal of the LSI chip, each of output terminal of the switch circuits being connected to one of the test signal output terminals, each of control terminals of the switches being connected to one of the output bits of the shift register,

each switch circuit having a second number of switches, each of which includes an input terminal, an output terminal and a control terminal, each input terminal of the switches being connected to one of the input terminals of its switch circuit,

each output terminal of the switches being connected to one of the output terminal of its switch circuit, and the each control terminal of the switches being commonly connected to the control terminal of its switch circuit.

Claim 5 (withdrawn). An LSI chip as claimed in claim 4 wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal.

Claim 6 (withdrawn). An LSI chip as claimed in claim 4 further including a clock input terminal, the clock input signal is inputted to the clock input terminal from an external device.

Claim 7 (withdrawn). An LSI chip as claimed in claim 4 wherein the number of output bits of the shift register being half of the first number, the second number being two and the number of the switch circuits being half of the first number.

Claim 8 (withdrawn). An LSI chip having a plurality of output terminals and a test circuit, the test circuit comprising:

a single test signal input terminal;

a single test signal output terminal;

a shift register having an input terminal, which is connected to the test signal input terminal, output bits of the shift register being half of a number of the output terminals of the LSI chip, and a voltage level of one of the output bits of the shift

register being different from these of other output bits of the shift register in response to a clock pulse;

a plurality of switches, each of which includes an input terminal, an output terminal and a control terminal, a number of the switches being half of the number of the output terminals of the LSI chip, each input terminal of the switches being connected to one of the output terminals of the LSI chip, the output terminals of the switches being commonly connected to the test signal output terminal, and each control terminal of the switches being connected to one of the output bits of the shift register;

an output polarity signal input terminal receiving an output polarity signal; and

an output circuit having output terminals and input terminals wherein each number of the output terminals and the input terminals equals that of the output terminals of the LSI chip, each of the output terminals being connected to one of the output terminals of the LSI chip, and the output circuit having a plurality of signal switching circuits wherein a number of signal switching circuits is half of the output terminal of the LSI chip, each of which includes,

a first input terminal and second input terminal and a first output terminal and a second output terminal, each of the first and second input terminals of each signal switching circuit being connected to one of the input terminals of the output circuit, the first output terminal of each signal switching circuit being connected to one of the output terminal of the of the LSI chip, which is connected to the switch, the second output terminal of each signal switching circuit being connected to one of the output terminal of the of the LSI chip, which is not connected to the switch, and,

wherein each signal switching circuit outputs a signal received at its first input terminal to its first output terminal while receiving the output polarity signal having a first voltage level at the output polarity signal input terminal, and outputs a signal received at its second input terminal to its first output terminal while receiving the output polarity signal having a second voltage level, which is different from the first voltage level, at the output polarity signal input terminal.

Claim 9 (withdrawn). An LSI chip as claimed in claim 8 wherein the LSI chip is an analog voltage output driver LSI chip, and each output terminal of the analog voltage output driver LSI chip outputs an analog voltage signal.

Claim 10 (withdrawn). An LSI chip as claimed in claim 8 further including a clock input terminal, the clock input signal is inputted to the clock input terminal from an external device.

Claim 11 (withdrawn). An LSI chip as claimed in claim 8, wherein each signal switching circuit further including:

a first output amplifier whose input terminal is connected to the first input terminal of the signal switching circuit;

a second output amplifier whose input terminal is connected to the second input terminal of the signal switching circuit;

a first selector whose input terminal is connected to an output terminal of the first output amplifier and whose output terminal is connected to the first and second output terminals of the signal switching circuit; and

a second selector whose input terminal is connected to an output terminal of the second output amplifier and whose output terminal is connected to the first and second output terminals of the signal switching circuit,

wherein the first selector electrically connects its output terminal to the first output terminals of the signal switching circuit in response to the output polarity signal having a first voltage level, and wherein the second selector electrically connects its output terminal to the first output terminals of the signal switching circuit in response to the output polarity signal having a second voltage level.

Claim 12 (currently amended). A chip carrier, which has a user area and a non-user area, for mounting a LSI chip in the user area, comprising:

a plurality of input leads, each of which is formed in the user area and extended in a first direction to the non-user area;

a plurality of output leads, each of which is formed in the user area and extended in a second direction, which is different from the first direction, to the non-user area;

a single test signal input lead, which is formed in the user area and extended in the first direction to the non-user area, the single test signal input lead receiving a test signal for testing an internal circuit formed in the LSI chip; and

a single test signal output lead, which is formed in the user area and extended in the first direction to the non-user area, the ingle test signal output lead outputting a test signal only.

Claim 13 (original). A chip carrier as claimed in claim 12, further comprising a plurality of test pads formed in the non-user area, each of which is connected to one of the output leads.

Claim 14 (original). A chip carrier as claim in claim 12 wherein a width of the test signal output lead is wider than that of each output lead.

Claim 15 (currently amended). A chip carrier as claim in claim ~~11~~ 12 wherein the test signal input lead and the test signal output lead sandwich the input leads.

Claim 16 (withdrawn). A chip carrier, which has a user area and a non-user area, for mounting a LSI chip in the user area, comprising:

a plurality of input leads, each of which is formed in the user area and extended in a first direction to the non-user area;

a plurality of output leads, each of which is formed in the user area and extended in a second direction, which is different from the first direction, to the non-user area;

a single test signal input lead, which is formed in the user area and extended in the first direction to the non-user area; and

at least two test signal output leads, each of which is formed in the user area and extended in the first direction to the non-user area.

Claim 17 (withdrawn).A chip carrier as claimed in claim 16, further comprising a plurality of test pads formed in the non-user area, each of which is connected to one of the output leads

Claim 18 (withdrawn).A chip carrier as claim in claim 16 wherein a width of each test signal output leads is wider than that of each output lead.

Claim 19 (withdrawn).A chip carrier as claim in claim 16 wherein the test signal input lead and the test signal output leads sandwich the input leads.